ABSTRACT OF THE DISCLOSURE

A vector information processing apparatus has a CPU comprising a plurality of asynchronously operating units, a main memory for storing data, and a main memory

5 controller for controlling the writing of data in the main memory. The main memory controller has a VSC address buffer for holding a storage address in the main memory for each element designated by a vector scatter instruction. The main memory controller is arranged to

10 inhibit the outputting of a writing permission signal for the main memory which is generated according to a writing request for writing an element having a smaller element number, which has the same storage address as the storage address and which has not been processed in

15 a sequence of element numbers, of writing requests for writing elements in the main memory which are issued respectively from the asynchronously operating units according to a vector scatter instruction.

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